كلية الهندسة
College of Engineering
QATAR UNIVERSITY جامعة قطر

EE SEMINAR SERIES

Speaker's Bio:

Prof. Sofiène Tahar received in 1990 the Diploma degree in computer engineering from the University of Darmstadt, Germany, and in 1994 the Ph.D. degree with "Distinction" in computer science from the University of Karlsruhe, Germany.
Currently he is Professor in the Department of Electrical and Computer Engineering at Concordia University, Montreal, where he is holding a Senior Research Chair in Formal Verification of System-on-Chip.
Dr. Tahar is founder and director of the Hardware Verification Group (http://hvg.ece.concordia.ca) at Concordia University, which carried pioneering work in the past 15 years in collaboration with multinational industry and renowned research institutions.
Prof. Tahar has received several awards and distinctions, including in 2007 the title of Concordia University Fellow for being the best senior researcher of the year, and in 2010 a National Discovery Award provided to Canada's top 100 Engineering and Sciences researchers. Dr. Tahar is member of the Order of Engineers of Quebec, Senior member of IEEE and Senior member of ACM.

The Department of Electrical Engineering, cordially invites you to a seminar on

System-on-Chip Design Verification: Challenges and State-of-the-art

By

Prof. Sofiène Tahar

Date: Wednesday, April 24, 2013
Time: 11:00 am - 12:00 pm
Venue: G-209

Abstract

A System-on-Chip (SoC) is an integrated circuit composed of heterogeneous components ranging from microprocessors, digital, analog, RF, embedded memory to optical, MEMS and even biometric devices. The verification of an SoC is a very challenging task in terms of human, computer and budget resources. Many product delays are caused by verification taking longer than expected, and despite multiple efforts, products are delivered with uncaught bugs. During the seminar, I will review some of the challenges faced with SoC verification, where several technologies (analog/digital/optical) have to be modeled and verified at both block and system levels. Several technologies will be displayed and compared, drawing a picture to still open problems and possible research issues. Among them "formal verification" is one of the most active areas that is carried out since recently and which make use of computerized mathematical reasoning to verify system properties. Some of these techniques will be elaborated with example projects carried out by my research group at Concordia University (http://hvg.ece.concordia.ca), which activities will also be briefly introduced during the seminar.